DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 24, 2007, has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. **Claims 9, 11 and 14** are rejected under 35 U.S.C. 103(a) as obvious over **Shimamoto et al. (US 2004/0188762**; previously cited**)** in view of **Wang et al. (US 2003/0181012**; previously cited**)**.

Regarding **claim 9, Shimamoto** discloses a manufacturing method of a semiconductor device **(FIGs. 2-4)** comprising the steps of:

forming a gate insulation film **(3 and 4, FIG. 2; pg. 3: [0052])**, over a silicon substrate **(1, FIG. 2; pg. 3: [0053])**; and

forming a gate electrode **(5, FIG. 3; pg. 3, [0057])**, over said gate insulation film **(3 and 4)**, said step of forming a gate insulation film including the steps of:

forming a silicon oxide film **(pg. 3: [0054])** over said silicon substrate **(1, FIG. 2)**, said silicon oxide film having a thickness of 1.5 nm or less **(pg. 3: [0054])**; and

introducing nitrogen into said silicon oxide film **(pg. 3: [0054])** and displacing silicon atoms on a surface of said silicon substrate toward said gate insulation film side; and

forming a high dielectric film constant film **(4; pg. 3: [0055], pg. 4: [0063])** over said nitrogen-introduced silicon oxide film **(3)** by a deposition method without oxidation of said nitrogen-introduced silicon film **(pg. 3: [0055], pg. 4: [0063]-[0064])**, immediately after said step of introducing nitrogen and displacing silicon atoms **(pg. 3: [0054])**.

Regarding the functional limitation of "displacing silicon atoms on a surface of said silicon substrate toward said gate insulation film side," **Shimamoto** discloses that nitrogen is introduced into said silicon oxide film by the thermal treatment in an NO (nitrogen monoxide) or N_2O atmosphere. It is well known that thermal treatment of silicon oxide in a nitrogen monoxide atmosphere, will displace the silicon atoms on a surface of a silicon substrate, toward the gate insulation film side.

Thus, **Shimamoto** teaches all the limitations of the claim with the exception of disclosing wherein said step of introducing nitrogen and displacing silicon atoms is done by conducting a heat treatment to said silicon oxide film in an ammonia atmosphere.

However, **Wang** teaches a method of making a semiconductor device wherein a gate insulation film is formed by introducing nitrogen into a silicon oxide film, wherein the nitrogen is introduced by conducting a heat treatment to the silicon oxide film in an

ammonia (NH_3) atmosphere **(pg. 4: [0047])**. Furthermore, regarding the limitation of "displacing silicon atoms on a surface of said silicon substrate toward said gate insulation film side," **Wang** teaches a method substantially identical to that of the applicant's, for introducing nitrogen into a silicon oxide film, which causes the displacement of silicon atoms on said silicon substrate **(pg. 4: [0047])**. Therefore, since the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a prima facie case of obviousness has been established. *In re Best*, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of **Wang** into the method of **Shimamoto**, thereby, conducting the heat treatment in ammonia (NH_3) atmosphere rather than nitrogen monoxide (NO) or nitrous oxide (N_2O). **Wang** discloses that NH_3 nitridation treatment, compared to N_2O nitridation, effectively introduces the nitrogen into the oxide, increases the dielectric constant, and keeps the physical thickness of the oxide unchanged **(Wang: pg. 4, ¶ [0048])**.

Regarding **claim 11, Shimamoto** discloses the method wherein said gate insulation film is formed over a region where a conductive type of said surface of said silicon substrate is P-type **(pg. 3: [0051]-[0053])**.

Regarding **claim 14, Wang** discloses the method wherein said heat treatment is conducted at 775 degree C or higher **("900°C," pg. 4: [0047])**.

Response to Arguments

2. Applicant's arguments with respect to claims 9, 11 and 14, filed on September 24, 2007, have been considered but are moot in view of the new ground(s) of rejection.

Although Applicant's arguments are moot, in light of the new grounds of rejection, Applicant's arguments regarding the Wang reference will be discussed to further explain the Office's position.

With respect to the Wang reference Applicant states: "In Wang, silicon atoms are never displaced because nitriding is conducted to a thick oxide film." The argument is not persuasive, because Wang teaches a thin oxide film of 1.5-1.8 nm ("15-18 Á," pg. 4: ¶ [0047]). Furthermore, note that the thickness range taught by Wang overlaps the "thickness of 1.5 nm or less," recited by the Applicant in claim 9.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abul Kalam whose telephone number is 571-272-8346. The examiner can normally be reached on Monday - Friday, 9 AM - 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. K./

/Phat X Cao/
Primary Examiner, Art Unit 2814